Evaluation of ultra-thin structures composed of graphene and high-k dielectrics for resistive switching memory applications

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Abstract

Nowadays the electronic industry is reaching a point that in order to keep up with the Moore's law is necessary the introduction of novel materials and think about new kind of architectures. This is especially important in memory applications, as the present non-volatile memory technology soon will have to be replaced by an alternative. One option is the Resistive Random Access Memory (RRAM) technology [1], based in the formation and destruction of conductive filaments (CF) in insulators [2], being this phenomenon called Resistive Switching (RS). By using high-k dielectrics like HfO_2 in a future will be possible to integrate this technology at industrial level, as the fabrication of these structures follows the same CMOS fabrication process like the silicon technology. Moreover, the combination of this technology with other novel materials, like graphene [3], could boost its performance.

In this work, prototypes of structures composed of graphene and ultrathin polycrystalline HfO_2 are evaluated (Fig.1a) for memory applications. First of all, polycrystalline HfO_2 of 5 nm was fabricated by Atomic Layer Deposition (ALD) over silicon substrates. Graphene grown by the Chemical Vapour Deposition (CVD) method is transferred over the substrate by the standard procedure. Then, Au/Ti square shaped electrodes of 80x80 μm^2 are fabricated using photolithography techniques. Finally the samples were etched by O_2 plasma using a Reactive Ion Etching (RIE) process in order to eliminate the graphene material that not is underneath the metal electrodes (Fig. 1b). Samples without graphene were also prepared, which are considered as reference. Then the samples were electrically analysed using a 4-probe station.

The electrical analysis of the reference samples show that the capacitor structure reaches high current levels (of μA) even at low voltages (Fig. 2a), suggesting the existence of conductive paths even without any forming process. These conductive paths, which didn't show any RS phenomenology, could be related to the presence of grain boundaries, due the high cristanillity of the sample, which were already observed to be leaky sites in Metal-Insulator-Semiconductor (MIS) structures based on such dielectrics [4]. On the other hand, on the structures with graphene between the top electrode and the HfO_2 layer, the device is somehow protected and currents of μA are only reached (Fig. 2b) when forming voltages of ~5V are applied. These results indicate that graphene may favour in some cases the control of the CFs present in the dielectric, and ultimately the RS phenomenon.

References

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Figures

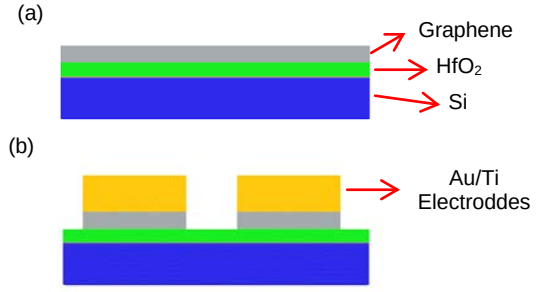

Fig 1. (a) Scheme of the Graphene/HfO_2/Si structures fabricated. (b) Final device configuration.

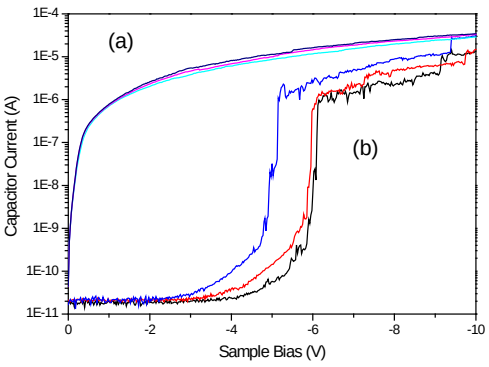

Fig 2. (a) Curves obtained from the structures without graphene and (b) with graphene.